Amendments to the Specification:

Please replace paragraph [0001] with the following amended paragraph:

[0001] This application claims priority under 35 USC ~~§ 119(e)(1)~~ §119(e)(1) of Provisional Application No. 60/452,397, filed March 6, 2003.

Please replace paragraph [0004] with the following amended paragraph:

[0004] Each PCM audio signal ~~samples~~ sample on a CD ~~are translated into 16 bits representing the~~ that represents a value of the analog audio signal is 16 bits in length. PCM signals have a uniform time period between samples, with the rate of sampling varying from 4 KiloHertz (KHz) to 192 KHz. DSD signals are sampled at much higher rates such as 2.8224 MegaHertz (MHz). Thus, an audio signal sampled using a PCM system at 44.1 KHz sampling rate and a DSD system at 2.8224 MHz sampling rate would result in 64 DSD samples occurring between each PCM sample.

Please replace paragraph [0005] with the following amended paragraph:

[0005] Sampling an analog audio signal into a DSD signal may be performed by a sigma-delta modulator. A sigma-delta modulator includes analog circuitry that captures the analog audio signal and converts it into a single bit stream. Because of its single bit format, DSD signals can be converted back into the analog audio signal using minimal hardware. However, manipulation of the single bit DSD stream representing the analog audio signal can be very difficult. For example, tasks such as increasing the volume, adjusting treble or bass, ~~etc.~~ etc., is very difficult because the DSD signal cannot be easily processed using existing digital filters and digital signal processing ~~(DSP)~~ techniques. One solution is to convert the DSD signal into a PCM signal using a Finite Impulse Response (FIR) digital filter. PCM signals can be processed using digital filters and DSP techniques to allow manipulation of the PCM signal to accomplish tasks such as increasing the volume or adjusting bass and for more complex tasks such as

surround sound effects. After manipulation of the PCM signal, the signal may be converted back to a DSD signal and/or into analog audio signal format ~~and transmit~~ for output to speakers.

Please replace paragraph [0006] with the following amended paragraph:

[0006] Conversion of the DSD signal to a PCM signal may require a high quality and expensive FIR digital filter containing large quantities of complex hardware. The DSD to PCM converter may have an odd sized binary multiplier for multiplying 1 bit by the number of bits needed to encode the PCM signal (i.e. 1 by 16 bit multiplier, 1 by 24 bit multiplier, 1 by 32 bit multiplier, ~~and so on...~~ etc.). The DSD to PCM converter may also include a sign controller and an N-coefficient buffer to implement the FIR filter.

Please replace paragraph [0007] with the following amended paragraph:

[0007] Digital signal processors (DSPs) that do not contain the dedicated hardware described above for DSD to PCM conversion are not capable of efficiently performing this conversion. Thus, there has been a longfelt need for an improved and low-cost method implemented in software or firmware and apparatus for efficient conversion of DSD signals to PCM signals in a ~~digital signal processor (DSP)~~ DSP.

Please replace paragraph [0013] with the following amended paragraph:

[0013] The present invention provides significant advantages over the prior art. One advantage is the simplified circuitry and elimination of special hardware (~~e.g.~~ e.g., 1 bit by 32 bit multiplier) for conversion of DSD signals to PCM signals. Another advantage is the reduced processor resources and bandwidth needed to convert signals using the present invention. The apparatus and method of the present invention can process multiple DSD sample bits (~~e.g.~~ e.g., 16 bits, 32 bits, 64 bits, and so on) to a PCM signal sample in one clock cycle resulting in much faster conversion. Finally, because the present invention may be implemented in firmware or

software, another advantage is that modifications to the firmware or software code can be easily and quickly performed.

Please replace paragraph [0016] with the following amended paragraph:

[0016] DSD to PCM signal conversion device **100** also includes an *N*-coefficient buffer **120**. The *N*-coefficient buffer includes coefficients c1 **125a**, c2 **125b**, c3 **125c**, ..., and cN **125N** that are each 32 bits in length **124**. Coefficients c1 to cN are general FIR low pass filter coefficients derived using well known ~~general~~ methods. The resulting coefficients c1 to cN in the coefficient buffer are used to multiply each coefficient by its corresponding DSD signal bit value over a period of time, as described below, to generate the correct values to reproduce the analog audio signal.

Please replace paragraph [0017] with the following amended paragraph:

[0017] Each bit in the *N*-bit delay line has a corresponding coefficient in the *N*-coefficient buffer. Thus, the most significant bit **105** in the *N*-bit delay line **110** corresponds to coefficient c1 **125a** in the *N*-coefficient buffer **120**. An address generator ~~**110**~~ **115** moves from left to right and sequentially accesses each bit in the *N*-bit delay line **110**. For each bit in the *N*-bit delay line **110**, the address generator ~~**110**~~ **115** determines the corresponding coefficient in the *N*-coefficient buffer **120**. Sign controller **130** receives the bit value of the *N*-bit delay line **110** currently accessed by the address generator ~~**110**~~ **115** and sets output line **133** high or low depending on whether the bit value is one or zero.

Please replace paragraph [0019] with the following amended paragraph:

[0019] Alternatively, the sign controller ~~**130**~~ may connect to the multiplier MPY ~~**135**~~ through a 32 bit bus (not shown). The sign controller **130** may provide -to the multiplier MPY **135** a binary 32 bit value of decimal +1.0 or -1.0 depending on whether the bit value from *N*-bit delay line **110** is one or zero, respectively. In this system, multiplier MPY **135** performs a 32 bit

by 32 bit multiply with the output from sign controller **130** and coefficient **125** from *N*-coefficient buffer **120**. The multiplier MPY **135** sends the result of the multiplication via 32 bit output bus **140** to adder **150**.

Please replace paragraph [0020] with the following amended paragraph:

[0020] Accumulator **170** couples to adder **150** through 32 bit bus **160** and initially contains a zero value. The current 32 bit value contained in the accumulator **170** is fed back to the adder **150** through bus 155 to be summed with the next output from multiplier MPY **135**. The result of this addition is then loaded into accumulator **170** and then summed with the next output from multiplier MPY **135**. Once all bits have been processed in the *N*-bit delay line **110** (i.e. the address generator has reached the least significant bit **185** in *N*-bit delay line **110**) the accumulator **170** contains a 32 bit PCM signal sample that it transmits through output bus **175**. The *N*-bit delay line **110** may then be loaded with the next *N* bit samples from the DSD signal for conversion to a PCM signal sample.

Please replace paragraph [0026] with the following amended paragraph:

[0026] The resulting 32 bit precomputed sum from the look-up table **260** for the corresponding word from FIFO buffer **205** is provided to output bus **235** and added in adder **240** to the current value of accumulator **255**. Preferably, accumulator **255** is initially set to a zero value. The current 32 bit value contained in the accumulator **255** is fed back to the adder **240** through bus **245** to be summed with the next 32 bit precomputed sum from look-up table **260**. The result of this addition is then loaded into accumulator **255** through bus **250** and then summed with the next output from look-up table **260**. Once all words have been processed in the current line **202** of the FIFO buffer **205** (i.e. the address generator has reached the least significant word **214** in FIFO buffer **205**) the accumulator **255** contains a 32 bit PCM signal sample **290** that it transmits through output bus **285**. The FIFO buffer **205** then flushes line **202** from the FIFO buffer and moves the next line below line **202** to the top of the FIFO buffer for conversion from DSD signal bits to a PCM signal sample.

Please replace paragraph [0031] with the following amended paragraph:

[0031] DSP **200** is now ready to receive DSD signal samples for conversion to multiple bit PCM signal samples using the generated look-up table as described with reference to flow chart **400** in Figure 4. Referring also to Figure 2, the FIFO buffer **205** receives N bits from the DSD signal, and flushes out the oldest N bits that have been converted to a multiple bit PCM signal sample as shown in block **420**. The N bits are subdivided into words corresponding to sections as shown in Figure 2. The address generator **220** starting at the most significant word **212** and traversing sequentially from left to right to access each word, determines the correct precomputed sum by performing a look-up in table **260** to match the bit pattern in word to the correct bit pattern 00..00b **276a** ... 11..11b **276n**. Thus, after the variables section and sum are initially set to zero in block **440** **430**, a look-up of the two dimensional array table[section][word[section]] containing the precomputed sums is performed and added to the sum in block **440**. In the two dimensional table array, word[section] corresponds to the bit pattern in the word. Thus, as shown in Figure 2 for section=0, word[section=0]=11001101b=205dec and element table[section=0][word[section=0]=205] contains the precomputed sum corresponding to word[0].

Please replace paragraph [0032] with the following amended paragraph:

[0032] After adding the precomputed sum for the word to sum, the variable section is incremented to determine the precomputed sum for the next word and this value is added to the sum variable. Thus, in block **450** after all words have been evaluated and the address generator has reached the section(N/n – 1) in the look up table **260** and corresponding word(N/n – 1) **214**, the condition is not true since section=N/n. Block **460** is evaluated and the multiple bit PCM signal sample in variable sum is ~~generated~~ output. Finally, in block **470** if input continues from the DSD signal, then N DSD samples are loaded into the FIFO buffer as given in block **420** and the oldest N bits are flushed out. If no more bits from the DSD signal are in the FIFO buffer for conversion to PCM signal samples, the conversion technique stops in block **480**.

Please replace paragraph [0033] with the following amended paragraph:

[0033] The technique described above for conversion of DSD signals to PCM signals reduces the sampling rate for the PCM signal samples. Thus, if the DSD signal is sampled at a rate of 2.8224 MHz and N DSD samples are converted to one PCM signal sample, the PCM signal sampling rate is decimated to 2.8224/N MHz. Common values of N=16, 32, and 64 would ~~given~~ yield respective sampling rates of 176.4 KHz, 88.2 KHz, and 44.1 KHz.